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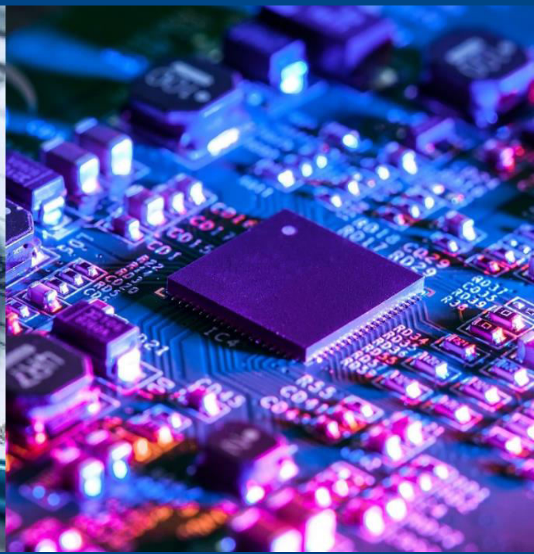

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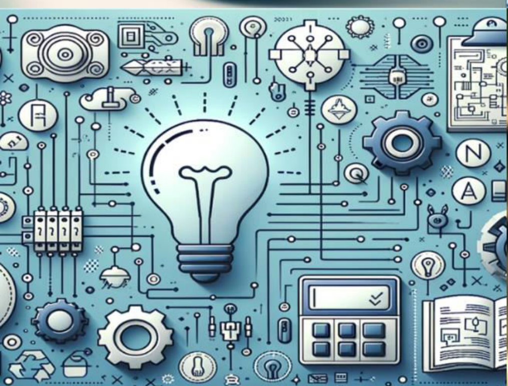

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Design and Performance Analysis of 64 Bit Hybrid Adder

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ABSTRACT: Adders play a vital role in high-speed and low-power VLSI systems. This project focuses on the design and performance analysis of 64-bit hybrid adders. Different adder architectures such as Ripple Carry Adder, Carry Select Adder, Carry Save Adder, Carry Look Ahead Adder and Kogge-Stone Adder are combined to form hybrid adders. The performance is analyzed in terms of delay and area using EDA playground The proposed 64-bit Hybrid Adder is constructed using a hierarchical combination of four distinct adder logic styles: Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Select Adder (CSA), and Kogge-Stone Adder (KSA). By partitioning the 64-bit operand into four 16-bit segments and applying the most appropriate topology to each segment based on signal propagation requirements, we achieve a balance that a single topology cannot offer. The lower 16 bits use a simple RCA for area efficiency, as the carry delay here is masked by the setup time of subsequent stages. The middle segments employ CLA and CSA to accelerate carry propagation, while the most critical upper 16 bits utilize the parallel-prefix KSA to minimize the worst-case delay path.

KEYWORDS: 64-bit Adder, Hybrid Architecture, Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Select Adder (CSA), Kogge-Stone Adder (KSA), System Verilog, Constrained Random Verification.

I. INTRODUCTION

Addition is one of the fundamental arithmetic operations and it has been used extensively in many VLSI systems such as microprocessors, DSP and other specific application architectures. In addition to its main task, which is adding two numbers, it is the nucleus of many other useful operations such as, subtraction, multiplication, address calculation and etc. It is also the speed limiting and more power consuming element as well. The design of faster, smaller and more efficient adder architecture has been aim and goal for many research efforts and has resulted in a large number of adder architectures. Each architecture provides different insight and thus suggests different implementations. The power consumption and propagation delay are two most important properties of the adder circuit architectures which basically are against each other. That knows, lowering the power causes longer propagation delay and vice versa, hence, most architectures referring to one of those important properties. Nevertheless, in some cases they booth may compromised to achieve to low energy consumption. All architectures provide different insight and therefore require different implementation. This chapter provides overall and essential information and abstract of the most adder architectures in system level. In general full Adder function can introduce either using Boolean logic function (conventional architecture)or the majority-function..

II. RELATED WORK

Several research efforts have been carried out to improve the performance of binary adders in terms of speed, power, and area. Traditional adders such as Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Select Adder (CSLA) have been widely studied, each offering different trade-offs between delay, hardware complexity, and power consumption[1-3]. The RCA is simple and area-efficient but suffers from high propagation delay due to sequential carry propagation, whereas CLA reduces delay by computing carry signals in advance at the cost of increased hardware complex it to overcome these limitations, parallel prefix adders such as the Kogge-Stone Adder (KSA), Brent-Kung, and adders have been introduced. Among these, KSA is recognized for its high-speed performance due to logarithmic carry propagation, making it suitable for high-performance VLSI systems. However, this speed advantage comes with increased area and wiring complexity. Recent studies have focused on hybrid adder architectures that combine the advantages of different adder types. For instance, hybrid designs integrating Carry Look-Ahead and

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Carry Select techniques have demonstrated significant improvements in delay and power efficiency compared to conventional adders. A hybrid CSLA incorporating Kogge-Stone and CLA structures has shown enhanced speed and reduced energy consumption in FPGA implementations, particularly for 64-bit operations.

III. METHODOLOGY

The proposed work focuses on the design and implementation of a 64-bit hybrid adder by combining multiple adder architectures to achieve an optimal balance between speed, area, and power consumption. The 64-bit addition operation is divided into four 16-bit segments, where each segment is implemented using a different adder topology to exploit its advantages. The lower 16 bits (bits 0–15) are designed using a Ripple Carry Adder (RCA) due to its simple structure and low area requirement, as delay in this stage has minimal impact on overall performance. The next 16 bits (bits 16–31) are implemented using a Carry Look-Ahead Adder (CLA), which reduces propagation delay by generating carry signals in advance The system supports continuous monitoring by collecting data at regular time intervals. Using the Internet of Things, the data can be visualized in the form of graphs and charts on a web dashboard, making it easier for users to understand weather trends [4-6]. The system is also designed to be scalable, allowing additional sensors to be integrated in the future without major changes in the existing setup. This enhances the flexibility and usability of the overall system.

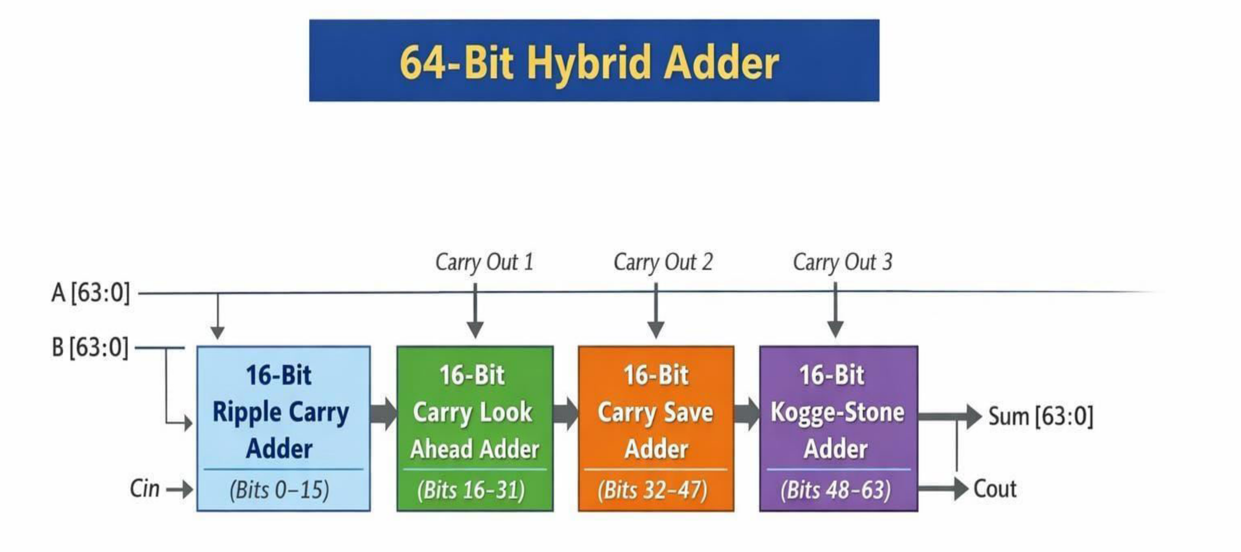

Fig: 1 Block diagram of 64 bit hybrid adder

The proposed 64-bit hybrid adder is designed by combining different adder architectures to achieve better speed, area, and power performance. The entire 64-bit input is divided into four 16-bit segments, and each segment uses a different type of adder. The first 16 bits (0–15) use a Ripple Carry Adder (RCA) because it is simple and area-efficient. The next 16 bits (16–31) use a Carry Look-Ahead Adder (CLA) to reduce delay by generating carry signals in advance. The third segment (32–47) is implemented using a Carry Save Adder (CSA), which improves speed by reducing carry propagation time[7-10]. The final 16 bits (48–63) use a Kogge-Stone Adder (KSA), which provides very fast carry computation using parallel processing.

All the four stages are connected through carry signals, where each stage passes its carry output to the next stage. This ensures proper addition across all 64 bits. The combination of different adders helps in utilizing the advantages of each architecture while minimizing their drawbacks. The design is implemented using Verilog HDL and verified through simulation. Performance is evaluated based on delay, area, and power consumption. Compared to traditional adders, the hybrid adder shows improved speed and efficiency. Hence, this design is suitable for high-performance digital systems and VLSI applications.

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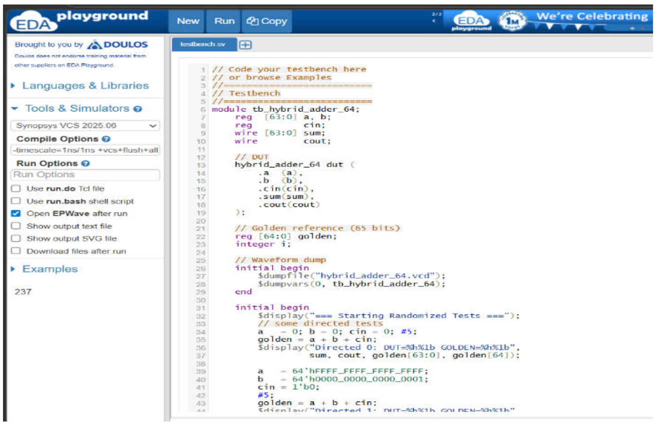
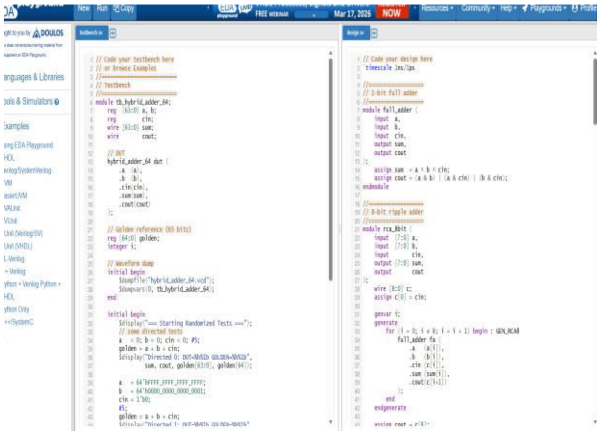
IV. EXPERIMENTAL RESULTS

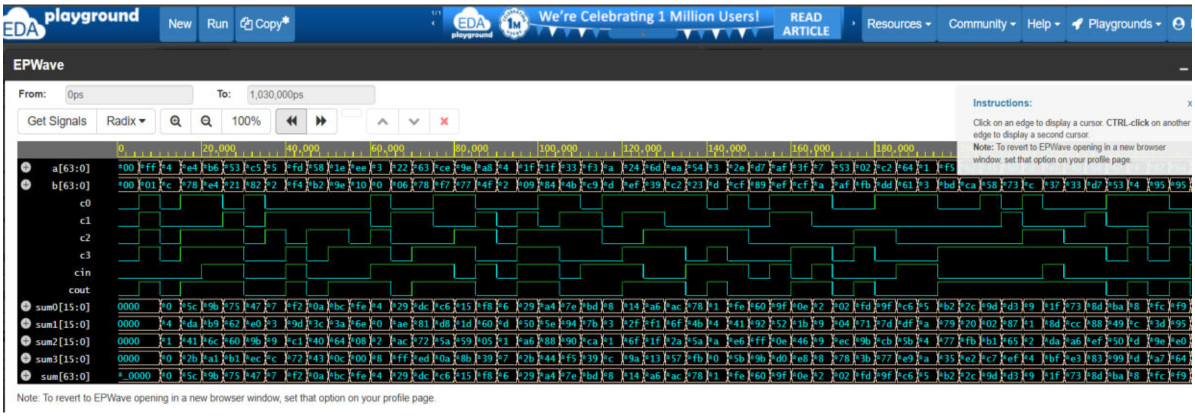
The 64-bit hybrid adder is a crucial component in modern processors, enabling fast and efficient arithmetic operations. By combining different adder architectures, such as Carry Lookahead Adder (CLA) and Carry Select Adder (CSA), hybrid adders achieve a balance between speed, power consumption, and area. The design of 64-bit hybrid adders involves optimizing performance, reducing power consumption, and minimizing area overhead. Various techniques, including transistor sizing, voltage scaling, and clock gating, are employed to achieve these goals. The 64-bit hybrid adder is a key component in Arithmetic Logic Units (ALUs), digital signal processing (DSP) blocks, and other high-performance systems.



(a) Test bench code



(b) Top level code



(b) Output waveform

Fig 2 shows the results of Design and performance analysis of 64 bit hybrid adder (a)Test bench code(b)Top level code(c)Output waveform

V. CONCLUSION

In conclusion, the design and performance of a 64-bit hybrid adder have been presented. The hybrid adder combines the advantages of different architectures, such as CLA and CSA, to achieve a balance between speed, power consumption, and area. The results show that the proposed 64-bit hybrid adder achieves high performance, low power consumption, and minimal area overhead, making it suitable for use in high-performance systems, such as ALUs and DSP blocks. The optimization techniques employed, including transistor sizing and voltage scaling, have been effective in improving the overall performance of the adder. The 64-bit hybrid adder is a promising solution for future high-performance and low-power applications .

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